

Specification for Mono OLED Display module

1.10" OLED Display module

Manufacturer	Truly Semiconductors LTD
Part n°	OEL9T0000-W-E
Ordering n°	OEL9T0000-W-E
Customer Part n°	n/a
Revision n°	1.0
Issue Date	2017/05/03

Customer's Approval

Company name	
Printed name	
Job title	
Signature	
Approval Stage:	This product is approved for the following production stage: -
	□ Pre-Production
	☐ Mass Production
Approval Date	

Supplied by Anders Electronics plc Manufactured by Truly Semiconductors LTD

SPECIFICATION

PART NO. : OEL9T0000-W-E



This specification may be changed without any notice in order to improve performance or quality etc.

Please contact OLED R&D department TRULY Semiconductors LTD. For updated specification and product status before design for this product or release the order.

Rev :1.0



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REVISION HISTORY

Rev.	Contents	Date
1.0	First release.	2017-05-03



■ PHYSICAL DATA

PHYSICAL DATA FOR OLED

No.	Items:	tems: Specification:			
1	Diagonal Size	1.1	Inch		
2	Resolution	196(H) x 96(V)	Dots		
3	Active Area	25.03 (W) x 11.22(H)	mm ²		
4	Outline Dimension (Panel)	30.08 (W) x 18.90(H)	mm ²		
5	Pixel Pitch	0.1171 (W) x 0.1278(H)	mm ²		
6	Pixel Size	0.0921(W) x 0.1028(H)	mm ²		
7	Driver IC	SSD1357	-		
8	Display Color	White	-		
9	Gray scale	1	Bit		
10	Interface	4-SPI/I ² C	-		
11	IC package type	COG	-		
12	Thickness	1.20±0.1	mm		
13	Weight	1.40±0.1	g		
14	Duty	1/96	-		

PHYSICAL DATA FOR TOUCH PANEL

No.	Items:	Specification:	Unit
1	Outline Dimension	33.70 (W) x 26.20 (H)	mm2
2	Driver IC	CP8CTST241	-
3	Construction	GF	-
3.1	First Layer	Strengthen Glass: 0.7	mm
3.2	Second Layer	OCA: 0.075	mm
3.3	Third Later	ITO film with sensor: 0.125	mm
4	Glass Material	Corning Gorilla 2320	-
5	Interface	I ² C	-
6	Surface Hardness	5H(Pressure 500 gf, 45 deg)	-
7	Surface Treatments	AF+AR	-
8	Weight	2.1 ± 0.1	g
9	Support points	1finger-touch+Gesture operation	-
10	Transmissivity	> 85%	@550nm

May. 03, 2017

■ ABSOLUTE MAXIMUM RATINGS

Unless otherwise specified, $V_{SS} = 0V$

 $(Ta = 25^{\circ}C)$

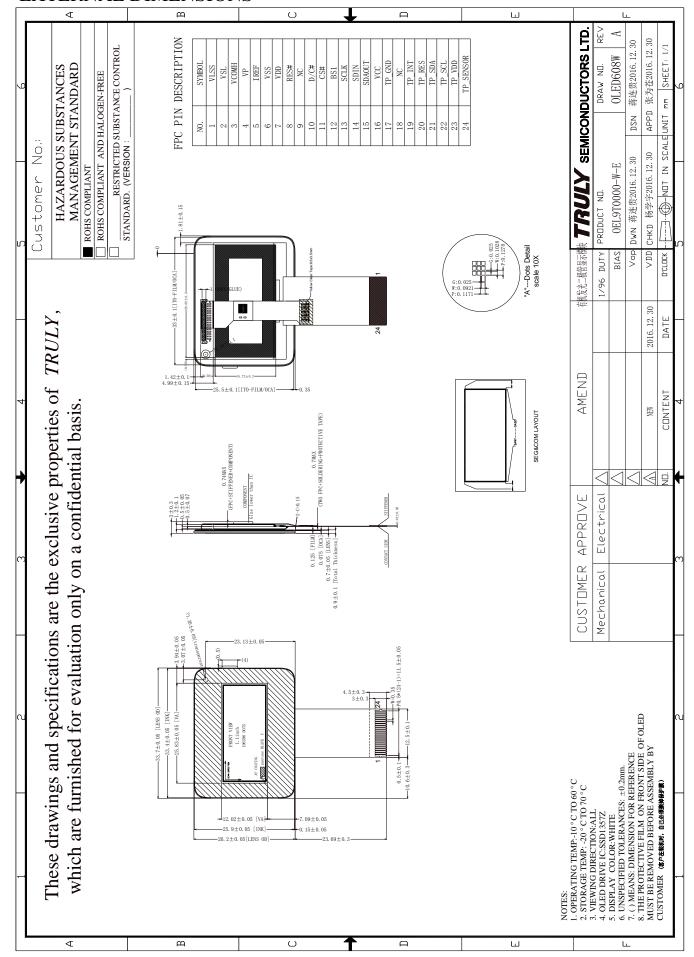
Items		Symbol	Min	Тур.	Max	Unit
Supply Voltage	Logio	VDD	-0.3	-	4.0	V
	Logic	TP_VDD	-0.5	-	6.0	V
	Driving	VCC	-0.5	-	19.0	V
Operating 7	Operating Temperature		-10	-	60	$^{\circ}$ C
Storage Temperature		Tst	-20	-	70	$^{\circ}$ C
Humidity(≤40°C)		-	1	-	90	%RH
Humidity(40~60°C)		-	1	-	60	%RH
Humidity(>60°C)		-	-	-	50	%RH

Note:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



■ EXTERNAL DIMENSIONS





■ ELECTRICAL CHARACTERISTICS

♦DC Characteristics

Unless otherwise specified, $V_{SS} = 0V$, VDD=1.65V to 3.5V.

 $(Ta = 25^{\circ}C)$

Items		Symbol	Min	Тур.	Max	Unit
	Logio	VDD	1.65	3.0	3.5	V
Supply Voltage	Logic	TP_VDD	1.71	2.1	5.5	V
Voltage	Driving	VCC	8.0	-	18.0	V
Input	High Voltage	V _{IH}	0.8 x VDD	-	VDD	V
Voltage Low Voltage		V _{IL}	0	-	0.2 x VDD	V
Output High Voltage		V _{OH}	0.9 x VDD	-	VDD	V
Voltage	Low Voltage	V_{OL}	0	-	0.1 x VDD	V

♦AC Characteristics

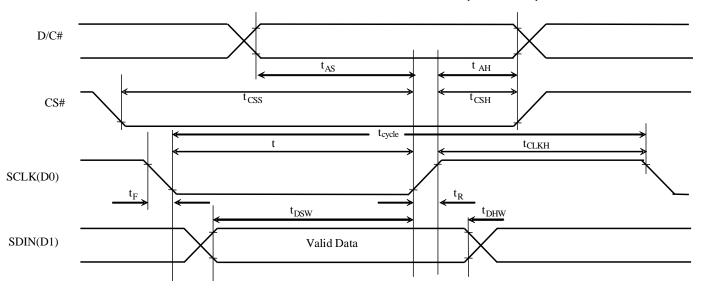
1. 4-wire Serial Interface Timing Characteristics

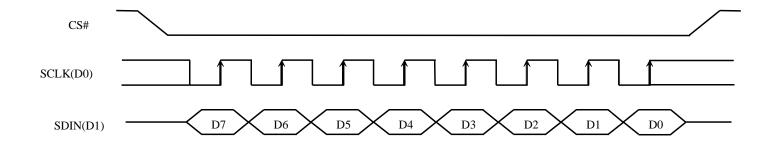
Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25 °C)

Symbol	Parameter	Min	Тур	Max	Unit
t _{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	42	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_{F}	Fall Time	-	-	15	ns

Serial interface characteristics (4-wire SPI)





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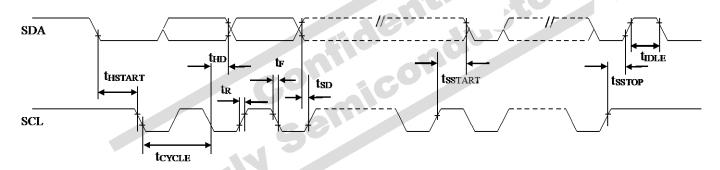
2. I²C Interface Timing Characteristics

I²C Interface Timing Characteristics

 $(V_{DD}-V_{SS}=1.65V \text{ to } 3.5V, T_A=25^{\circ}C)$

Symbol	Parameter	Min	Тур	Max	Unit
t _{cycle}	Clock Cycle Time	2.5	-	-	us
t _{HSTART}	Start condition Hold Time	0.6	-	-	us
t _{HD}	Data Hold Time (for "SDAout" pin)	0	-	-	ns
	Data Hold Time (for "SDA _{IN} " pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t _{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
tsstop	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t _F	Fall Time for data and clock pin	-	-	300	ns
t _{IDLE}	Idle Time before a new transmission can start	1.3	-	_	us

I²C interface Timing characteristics



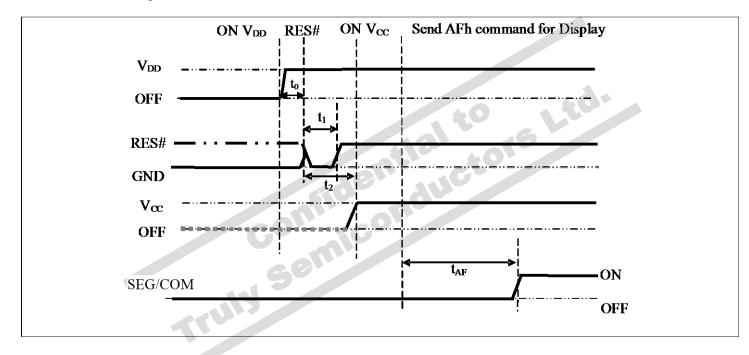
◆Power ON and OFF Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1357.

Power ON sequence:

- 1. Power ON V_{DD}
- 2. After V_{DD} become stable, wait at least 20ms (t₀), set RES# pin LOW (logic low) for at least 3us (t₁) ⁽⁴⁾ and then HIGH (logic high).
- 3. After set RES# pin LOW (logic low), wait for at least 3us (t₂). Then Power ON V_{CC}. (1)
- 4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).
- 5. After V_{DD} become stable, wait for at least 300ms to send command.

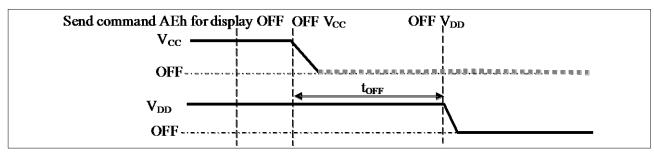
The Power ON sequence



Power OFF sequence:

- 1. Send command AEh for display OFF.
- 2. Power OFF V_{CC.}^{(1), (2)}
- 3. Power OFF V_{DD} after t_{OFF}. (4) (where Minimum t_{OFF}=0ms, typical t_{OFF}=100ms)

The Power OFF sequence



Note:

⁽¹⁾ V_{CC} should be kept float (i.e. disable) when it is OFF.

⁽²⁾ Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

⁽³⁾ The register values are reset after t₁.

 $^{^{(4)}}$ V_{DD} should not be Power OFF before V_{CC} Power OFF.

■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Items		Symbol	Min.	Тур.	Max.	Unit	Remark
Operating Lumi	nance	L	115	120*	-	cd/m2	White
Power Consum	ption	P	-	100	150	mW	30% pixels ON L=120cd/m ²
Frame Freque	ency	Fr	-	100	-	Hz	-
Color Coordinate	White	CIE x	0.260	0.290	0.320	CIE1931	Darkroom
Color Coordinate	Wille	CIE y	0.300	0.330	0.360	CILIFOI	
Dosmonso Timo	Rise	Tr	-	-	0.02	ms	-
Response Time	Decay	Td	-	-	0.02	ms	-
Contrast Ratio*		Cr	10000:1	-	-	-	Darkroom
Viewing Angle		Δθ	160	-	-	Degree	-
Operating Life	Γime*	Top	13,000	-	-	Hours	L=120cd/m2

Note:

- **1.** L=120 cd/m² is based on $V_{DD}=3.0V$, Vcc=13.0V, contrast command setting A:B:C = 0x7F:0x65:0x7F;
- 2. Contrast ratio is defined as follows:

Contrast ratio = Photo – detector output with OLED being "white"

Photo – detector output with OLED being "black"

3. Life Time is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternately displayed). (The initial value should be closed to the typical value after adjusting.)



■ INTERFACE PIN CONNECTIONS

No	Symbol	Description
1	VLSS	Analog system ground pin. It must be connected to external ground.
2	VSL	This is segment voltage (output low level) reference pin. This pin has to connect with resistor and diode to ground (details depends on application).
3	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.
4	VP	This pin is the segment pre-charge voltage reference pin. A capacitor can be connected between this pin and VSS to improve vision performance. No external power supply is allowed to connect to this pin.
5	IREF	This pin is the segment output current reference pin. IREF is supplied externally. A resistor should be connected between this pin and VSS to maintain the current around 10uA.
6	VSS	Ground pin. It must be connected to external ground.
7	VDD	Power supply pin for core logic operation. A capacitor should be connected between this pin and VSS.
8	RES#	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
9	NC	No connection.
10	D/C#	In 4-SPI mode, this pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at SDIN will be interpreted as data. When the pin is pulled LOW, the data at SDIN will be transferred to a command register. In I ² C mode, this pin acts as SA0 for slave address selection.
11	CS#	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
12	BS1	MCU bus interface selection pin. When the pin is pulled HIGH, the interface will be set as 4 line SPI. When the pin is pulled LOW, the interface will be set as I ² C
13	SCLK	Serial clock input
14	SDIN	Serial data input
15	SDAOUT	When I2C mode is selected, SDIN and SDAOUT should be tied together and serve as SDAout.
16	VCC	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. A capacitor should be connected between this pin and VSS.

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17	TP_GND	Ground pin for TP IC. It must be connected to external ground.
18	NC	No connection.
19	TP_INT	Interrupt pin for TP IC. Trigger a low level when touch occur.
20	TP_RES	Reset pin for TP IC. Restart TP by a GPIO of host CPU
21	TP_SDA	I ² C data input and output pin for TP IC.
22	TP_SCL	I ² C clock input pin for TP IC.
23	TP_VDD	Digital power supply for TP IC.
24	TP_SENSOR	Sensor pin for TP IC. Can be used to develop wrist operation function.



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■ COMMAND TABLE

(D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Funda	mental (Com	man	d Ta	ble						
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D 0	Command	Description
0 1 1	15 A[6:0] B[6:0]	0 *	0 A ₆ B ₆	0 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Column Address	A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	75 A[6:0] B[6:0]	0 *	1 A ₆ B ₆	1 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	$\begin{matrix} 0 \\ A_1 \\ B_1 \end{matrix}$	1 A ₀ B ₀	Set Row Address	A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0	5C 5D	0	1	0	1	1	1	0	0	Write RAM Command Read RAM Command	Enable MCU to write Data into RAM Enable MCU to read Data from RAM
0 1 1 1	A0 A[7:0] B[7:0]	1 A ₇ 0	0 A ₆ 0	1 A ₅ 0	0 A ₄ 0	0 A ₃ 0	0 A ₂ 0	0 A ₁ 0	0 A ₀ 0	Set Re-map / Color Depth (Display RAM to Panel)	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Column address 0 is mapped to SEG0 [reset] A[1]=1b, Column address 127 is mapped to SEG0 A[2]=0b, Color sequence: A → B → C [reset] A[2]=1b, Color sequence is swapped: C → B → A A[3]=0b, Reserved [reset] A[3]=1b, Reserved A[4]=0b, Scan from COM0 to COM[N → 1] [reset] A[4]=1b, Scan from COM[N-1] to COM0. Where N is the Multiplex ratio. A[5]=0b, Disable COM Split Odd Even A[5]=1b, Enable COM Split Odd Even [reset] A[7:6] Set Color Depth, 00b: 256color 01b: 65k color [reset] 10b: 262k color 11b Pseudo 262k color, 16-bit format 2 Refer to Product Preview Table 6-6 for details



Funda	mental (Com	man	d Ta	ble						
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A1 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Display Start Line	Set vertical scroll by RAM from 0~127. [reset=00h]
0	A2 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Display Offset	Set vertical scroll by Row from 0-127. [reset=00h]
0	A4~A7	1	0	1	0	0	1	X ₁	X_0	Set Display Mode	A4h: All OFF A5h: All ON (All pixels have GS63) A6h: Reset to normal display [reset] A7h: Inverse Display (GS0 -> GS63, GS1 -> GS62,)
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AEh = Sleep mode On (Display OFF) AFh = Sleep mode OFF (Display ON)
0 1	B1 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Sat Pasat	A[3:0] Phase 1 period of 2~30 DCLK(s) clocks [reset=0100b] A[3:0]: 0 invalid 1 = 2 DCLKs 2 = 4 DCLKs : 15 = 30DCLKs A[7:4] Phase 2 period of 2~30 DCLK(s) clocks [reset=1000b] A[7:4]: 0 invalid 1 = 2 DCLKs 2 = 4 DCLKs : 15 = 30DCLKs Note (1) 0 DCLK is invalid in phase 1 & phase 2



D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	Du	Command	Description
$\frac{0}{0}$	B3	1	0	1	1	0	0	1	1	Command	A[3:0] [reset=0000b], divide by DIVSET where
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
-	11[,10]	/	1 10	1 23	1 24	1 13	1 12	1	1 10		A[3:0] DIVSET
											0000 divide by 1
											0001 divide by 2
											0010 divide by 4
										Front Clock	0011 divide by 8
										Divider	0100 divide by 16
										(DivSet)/	0101 divide by 32
										Oscillator	0110 divide by 64
										Frequency	0111 divide by 128
											1000 divide by 256
											>=1001 invalid
0	D.	1						0			A[7:4] Oscillator frequency, frequency increases as level increases [reset=0010b]
0	B6	1	0	1	1	0	1	0	0		A[3:0] Set Second Pre-charge Period
1	A[3:0]	0	0	0	0	A_3	A_2	A_1	A_0		0000b invalid
											0001b 1 DCLKS
										Set Second Pre-	
										charge Period	A.C
										10	1000 8 DCLKS [reset]
										100	
									Ó		1111 15 DCLKS
0	B8	1	0	1	1	1	0	0	0	160	The next 63 data bytes define Gray Scale (GS) Table by
1			A1 ₆		_				· .		setting the gray scale pulse width in unit of DCLK's
1	A2[7:0]		$A2_6$						- 1		(ranges from 0d ~ 180d).
	A2[7.0]	A 27	A26	A25	A 24	A23	A_{2}	A_{21}	A 20		
1	•	•	•	•		1.1		•	•		A1[7:0]: Gamma Setting for GS1,
1	•	•									A2[7:0]: Gamma Setting for GS2,
1					1.60						: A62[7:0]: Gamma Setting for GS62,
1	A62[7:0]										A63[7:0]: Gamma Setting for GS63
1	A63[7:0]	A63 ₇	A63 ₆	A63 ₅	A63 ₄	$A63_3$	A63 ₂	A63 ₁	$A63_0$		1105[7.0]. Gamma Setting for GB03
										Master Look Up Table for Gray Scale Pulse width (Color A,B,C)	Note (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3 < Setting of GS62 < Setting of GS63 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input only, color A, B, C will follow the master LUT. (5) When command BCh is input, it selects individual LUT for color A, GS1~31A; When command BDh is input, it selects individual LUT for color C, GS1~31C (6) To select individual LUT for color B, A and C, comman B8h should be input before command BCh and BDh,



)/C#	Hex	D7	D6	D5	D4	D3	D2	D 1	D 0	Command		Desci	ription	
0	B9	1	0	1	1	1	0	0	1		Reset to default Lo	ok Up Tabl	e:	
											Color A	Color B		Color C
										Use Built-in	GS1A = 0 DCLK	GS1B = 0D	CLK	GS1C = 0 DCLK
										Linear LUT	GS2A = 4 DCLK	GS2B = 2D		GS2C = 4 DCLK
										[reset= linear]	GS3A = 8 DCLK	GS3B = 4D	CLK	GS3C = 8 DCLK
										[reset= inicar]	GS31A = 120 DCLK	GS62B = 12	2 DCLK	GS31C = 120 DCLF
												GS63B = 12	4 DCLK	
0	BB	1	0	1	1	1	0	1	1		Set pre-charge volta	age level.[r	eset = 111	[10b]
1	A[4:0]	0	0	0	A_4	\mathbf{A}_3	A_2	\mathbf{A}_1	A_0		454.03			T. 1
												Hex code		ge voltage
											00000	00h	0.10 x V	'cc
										Set Pre-charge	:		:	
											11110	1Eh	$0.50 \times V$	CC [reset]
										voltage	11111	1Fh	0.5133 x	V _{CC}
0	BC	1	0	1	1	1	1	0	0	. \$ 2	deselect voltage lev The next 31 data by		Gray Scal	e (GS) Table by
1			$A1_6$	_	_	_	_	_			setting the gray scale			
										100	(ranges from 0d ~ 1			
1	A2[7:0]	A2 ₇	A2 ₆	A2 ₅	A24	$A2_3$	AZ_2	$A2_1$	$A2_0$	70, 1	130			
1	•								37	-20	A1[7:0]: Gamma S	etting for C	SS1A,	
1								1.1			A2[7:0]: Gamma S	etting for C	SS2A,	
1										10	:			
1	A30[7:0]	A30-	A30-	A30-	A30.	A30°	A30 ₂	A30.	A30°		A62[7:0]: Gamma			
										Individual Look	A63[7:0]: Gamma	Setting for	GS31A	
1	A31[7:0]	A31 ₇	A31 ₆	A31 ₅	A314	A31 ₃	A31 ₂	A31 ₁	A31 ₀	Individual Look Up Table for				
										Gray Scale	Note			
					177					Pulse width	(1] 0 ≤Setting of GS	S1 < Setting	g of GS2 <	< Setting of GS3
										(Color A)	< Setting of GS30 <			
										(Colol A)	(2) GS0 does not ha	s pre-charg	e and curr	ent drive stages
											(3) GS1 can be set a	s only pre-	charge bu	t no current driv
											stage by input gan	nma setting	for GS1	equals 0.
											(4) When command			
											A, B and C. i.e. G			
											updated.	, -		
				ı	ı	1	1	1	ı					
											(5) Command B8h s	should be ir	put before	e command BCl



D/C#	Hex	D7	D6	D 5	D 4	D3	D 2	D 1	D 0	Command	Description		
D/C# 0 1 1 1 1 1 1	A2[7:0]	1 A1 ₇ A2 ₇		1 A1 ₅ A2 ₅	1 A1 ₄ A2 ₄	1 A1 ₃ A2 ₃	1 A1 ₂ A2 ₂	0 A1 ₁ A2 ₁	1 A1 ₀ A2 ₀	Command Individual Look Up Table for Gray Scale Pulse width	Description The next 31 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) for color C. A1[7:0]: Gamma Setting for GS1C, A2[7:0]: Gamma Setting for GS2C, : A62[7:0]: Gamma Setting for GS30C, A63[7:0]: Gamma Setting for GS31C Note (1) 0 ≤Setting of GS1 < Setting of GS2 < Setting of GS3		
										(Color C)	< Setting of GS30 < Setting of GS31 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input, it selects one LUT for colo A, B and C. i.e. GS1~31A, GS1~63B and GS1~31C are updated. (5) Command B8h should be input before command BCh and BDh to select individual LUT for color B, A and C.		
0	BE	1	0	1	1	1	1	1	0		Set COM deselect voltage level [reset = 05h]		
1	A[2:0]	0	0	0	0	0	A ₂	A ₁	A ₀	Set V _{COMH} Voltage	A[2:0] Hex code V COMH 000 00h 0.72 x Vcc : : : 101 05h 0.82 x Vcc [reset] : : : 111 07h 0.86 x Vcc		
0	C1	1	1	0	0	0	0	0	1		A[7:0] Contrast Value Color A [reset=7Fh]		
1	A[7:0]	A ₇			A_4				A_0	Set Contrast	B[7:0] Contrast Value Color B [reset=7Fh] C[7:0] Contrast Value Color C [reset=7Fh]		
1	B[7:0] C[7:0]	B ₇ C ₇	B ₆ C ₆	B ₅ C ₅	B ₄ C ₄	B ₃ C ₃	\mathbf{B}_2 \mathbf{C}_2	\mathbf{B}_1 \mathbf{C}_1	\mathbf{B}_0 \mathbf{C}_0	Current for Color A,B,C			
0	C7 A[3:0]	1 *	1 *	0 *	0 *	0 A ₃	1 A ₂	1 A ₁	1 A ₀	Master Contrast Current Control	A[3:0]: 0000b reduce output currents for all colors to 1/16 0001b reduce output currents for all colors to 2/16 1110b reduce output currents for all colors to 15/16 1111b no change [reset]		
0	CA	1	1	0	0	1	0	1	0		A[6:0] MUX ratio 4MUX ~ 128MUX, [reset=127], (Range		
1	A[6:0]	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Set MUX Ratio	from 3 to 127)		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation		

Funda	mental (Com	man	d Ta	ble						
D /C#	Hex	D7	D6	D5	D4	D3	D2	D 1	D 0	Command	Description
0	FD	1	1	1	1	1	1	0	1		A[7:0]: MCU protection status [reset = 12h]
1	A[7:0]	A ₇	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:0] = 12h, Unlock OLED driver IC MCU interface from entering command [reset]
										Set Command Lock	A[7:0] = 16h, Lock OLED driver IC MCU interface from entering command
											Note (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.

Note

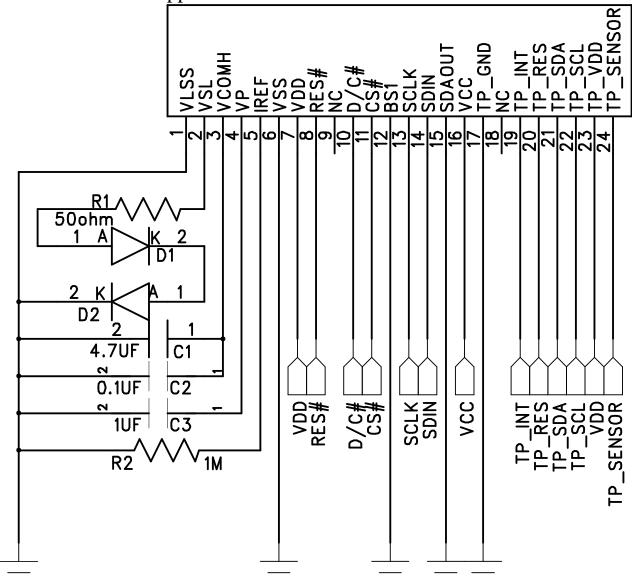
(1) "*" stands for "Don't care".

■ INITIALIZATION CODE

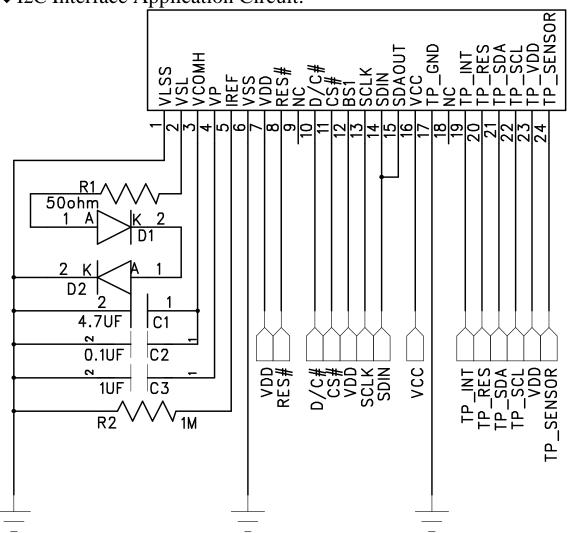
```
void InitOLED_SSD1357(void)
                                /* IC initialization function */
  Write_Command(0xAE);
                              //Sleep mode On (Display OFF)
                              //Set Re-map / Color Depth (Display RAM to Panel)
  Write_Command(0xA0);
  Write_Data(0xA4);
                              //262k color
                              //Enable COM Split Odd Even
                              //Color sequence is swapped: C->B->A
                              //Set Display Start Line
  Write_Command(0xA1);
  Write_Data(0x00);
  Write_Command(0xA2);
                              //Set Display Offset
  Write_Data(0);
  Write_Command(0xA6);
                              //Reset to normal display
  Write_Command(0xB1);
                              //Set Reset (Phase 1)/Pre-charge (Phase 2) period
  Write_Data(0x84);
                              //8 DCLKs/16 DCLKs
  Write_Command(0xB3);
                              //Front Clock Divider (DivSet)/Oscillator Frequency
  Write_Data(0x00);
                              //divide by 1
  Write_Command(0xB6);
                              //Set Second Pre-charge Period
  Write_Data(0x08);
                              //8 DCLKS
  Write_Command(0xB9);
                              //Use Built-in Linear LUT [reset= linear]
  Write_Command(0xBB);
                              //Set Pre-charge voltage
                              //0.50 \times VCC
  Write_Data(0x1E);
  Write_Command(0xBE);
                              //Set VCOMH Voltage
  Write_Data(0x05);
                              //0.82 \times VCC
  Write_Command(0xC1);
                             //Set Contrast Current for Color A,B,C
  Write Data(CONTRAST A);//0x7F
  Write_Data(CONTRAST_B);//0x65
  Write_Data(CONTRAST_C);//0x7F
                              //Master Contrast Current Control
  Write_Command(0xC7);
  Write_Data(0x0F);
                              //no change
  Write_Command(0xCA);
                              //Set MUX Ratio
  Write_Data(0x5F);
                              //96 duty
  Write_Command(0xAF);
                              //Sleep mode OFF (Display ON)
}
```

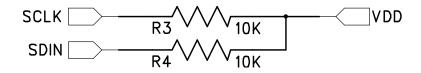
■ SCHEMATIC EXAMPLE

◆4-SPI Interface Application Circuit:









Note:

- (1) The values are recommended value. Select appropriate value against module application.
- (2) It is recommended to tie VLSS and VSS at one common ground point to minimize circulating ground noise.

■ RELIABILITY TESTS

	Item	Condition	Criterion				
High Te	emperature Storage (HTS)	70±2°€, 120 hours	 After testing, the function test is ok. After testing, no 				
High Ter	nperature Operating (HTO)	60±2°€, 96 hours	addition to the defect. 3. After testing, the change of luminance				
Low Te	emperature Storage (LTS)	-20±2°€, 120 hours	should be within +/- 50% of initial value. 4. After testing, the				
Low Ten	nperature Operating (LTO)	-10±2°€, 96 hours	change for the mono and area color must be within (+/-0.02, +/-				
High Tempe	erature / High Humidity Storage (HTHHS)	50±3°C, 90%±3%RH, 120 hours	0.02) and for the full color it must be within (+/-0.04, +/-0.04) of				
Thermal S	hock (Non-operation) (TS)	-20±2°C ~ 25°C ~ 70±2°C (30min) (5min) (30min) 10cycles	initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.				
Vibration (Packing) Drop (Packing)	10~55~10Hz,amplitu de 1.5mm, 1 hour for each direction x, y, z Height: 1 m, each time for 6 sides, 3 edges, 1 angle	One box for each test. No addition to the cosmetic and the electrical defects					
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF , 10times, air discharge)	 After testing, cosmetic and electrical defects should not happen. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting. 					

Note: 1) For each reliability test, the sample quantity is 3, and only for one test item.

- 2) The HTHHS test is requested the Pure Water(Resistance \geq 10M Ω).
- 3) The test should be done after 2 hours of recovery time in normal environment.

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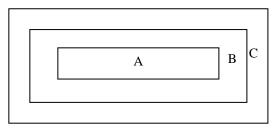
■ OUTGOING QUALITY CONTROL SPECIFICATION

♦Standard

According to GB/T2828.1-2003/ISO 2859-1: 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

♦ Definition

- 1 Major defect: The defect that greatly affect the usability of product.
- 2 Minor defect: The other defects, such as cosmetic defects, etc.
- 3 Definition of inspection zone:



Zone A: Active Area

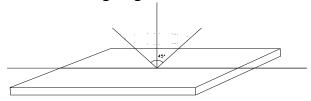
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer's product.

◆Inspection Methods

1 The general inspection: under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45 °viewing angle, under 25 ± 5 °C.



2 The luminance and color coordinate inspection: By PR705 or BM-7 or the equal equipments, in the dark room, under $25\pm5^{\circ}$ C.

◆Inspection Criteria

1 Major defect: AOL= 0.65

Item	Criterion
	1. No display or abnormal display is not accepted
Function Defect	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.



2 Minor Defect : AOL= 1.5

Minor Defect	: AQL= 1.5	2									
Item		Criterion	T								
~	Size ((mm)	Accepted Q	ty							
Spot Defect			Area A + Area B	Area C							
(dimming		Φ≦0.07	Ignored								
and	Y	$0.07 < \Phi \leq 0.10$	3								
lighting	X	0.10<Φ≦0.15	1	Ignored							
spot)		0.15<Φ	0								
	Note: $\Phi = (x + y) /$	2									
Line	L (Length): mm	W (Width): mm	Area A + Area B	Area C							
Defect	/	W ≤ 0.02	Ignored								
(dimming and	L≦3.0	$0.02 < W \le 0.03$	2								
lighting	L≦2.0	$0.03 < W \le 0.05$	1	Ignored							
line)	/	0.05 <w< td=""><td>As spot defect</td><td colspan="2"></td></w<>	As spot defect								
Polarizer Stain	Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and Line Defect.										
	1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.										
	2. If scratch can be seen only under non-operation or some special angle, the criterion is as below:										
Polarizer	L (Length): mm	W (Width): mm	Area A + Area B	Area C							
Scratch	/	W ≦ 0.02	Ignore								
	3.0 <l≦5.0< td=""><td>$0.02 < W \le 0.04$</td><td>2</td><td></td></l≦5.0<>	$0.02 < W \le 0.04$	2								
	L≦3.0	$0.04 < W \le 0.06$	1	Ignore							
	/	0.06 <w< td=""><td>0</td><td></td></w<>	0								
	Si	ze	Area A + Area B	Area C							
Dolomizon		Φ≦0.20	Ignored								
Polarizer Air Bubble	Y	$0.20 < \Phi \le 0.30$	2								
1 III 2 40010	X	$0.30 < \Phi \leq 0.50$	1	Ignored							
		0.50<Φ	0								



	,
	1. On the corner (mm)
Glass	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
Defect (Glass Chiped)	(mm) $x \leq a/4$ $y \leq s/3 \& \leq 0.7$ $z \leq t$
	3. On the other edges
TCP Defect	Crack, deep fold and deep pressure mark on the TCP are not accepted
Pixel Size	The tolerance of display pixel dimension should be within ±20% of the spec
Luminance	Refer to the spec or the reference sample
Color	Refer to the spec or the reference sample

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

- 1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
 - i. Avoid drop from high, avoid excessive impact and pressure.
 - ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
 - iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
 - iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
 - v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
 - vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
- 2. Do not attempt to disassemble or process the OLED Module.
- 3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
- 4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
- 5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
- 6. Be careful to prevent damage by static electricity:
 - i. Be sure to ground the body when handling the OLED Modules.
 - ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
 - iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
 - iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
 - v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
 - vi. Be sure to use anti-static package.
- 7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
- 8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
- 9. When the logic circuit power is off, do not apply the input signals.
- 10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
- 11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module's life time, even make it damaged.
- 12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

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13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$.

2. Soldering time: 3-4 sec.

3. Repeating time: no more than 3 times.

4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

♦ Precautions For Storing OLED Module:

- 1. Be sure to store the OLED Module in the vacuum bag with dessicant.
- 2. If the Module cannot be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
- 3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
- 4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
- 5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

♦ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

- 1. No warranty in the case that the precautions are disregarded.
- 2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

♦PRIOR CONSULT MATTER

- 1. For TRULY standard products, we keep the right to change material ,process ... for improving the product property without any notice on our customer.
- 2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.